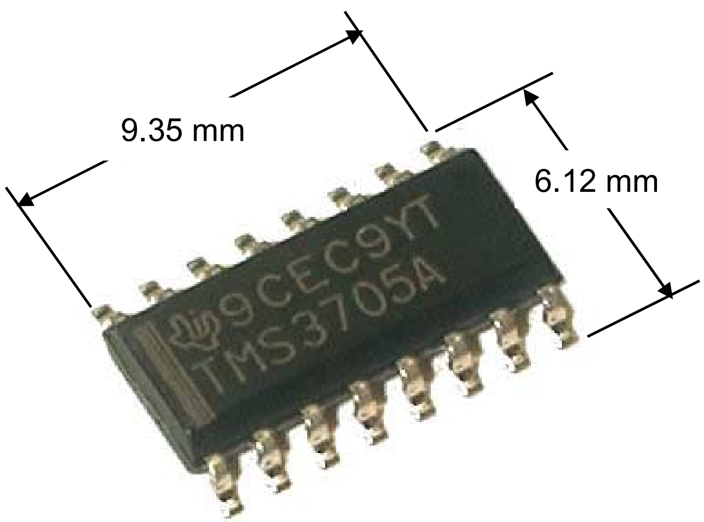
LF Technical Training

TMS3705A Transceiver IC

TMS3705A Transceiver IC Integration

4 Main Features



16 Pin SO Package

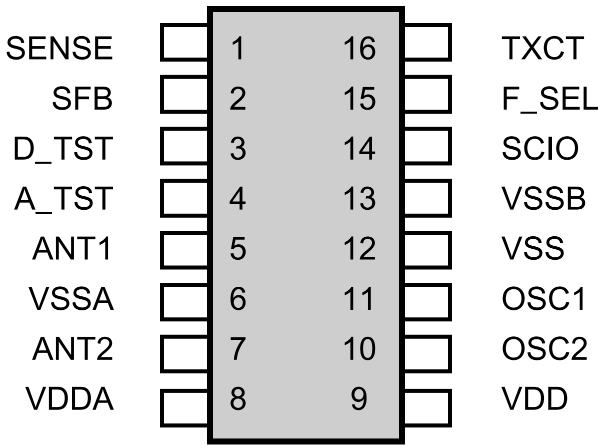
- 5V device
- Automatic sleep mode (TXCT idle for 100 ms)
- Transponder resonance frequency measurement
- Internal Full Bridge antenna driver
- Digital demodulator
- Diagnosis function
- Several operating modes
  - self adapting or fixed frequency charge-up
  - automatic or fixed demodulator threshold
  - asynchronous or synchronous data to µP
- Reduced additional component count
- PLL for internal clock generation
- 2/4 MHz crystal or low cost ceramic resonator can be used

TMS3705A Transceiver IC Integration

4 A Transceiver Module with antenna

4 Pin Names & Functions

D Package
(Top view)



PIN	NAME	I/O	DESCRIPTION
1	SENSE	I	Input of RF amplifier
2	SFB	O	Output of RF amplifier
3	D_TST	O	Test output for digital signals
4	A_TST	O	Test output for analog signals
5	ANT1	O	Antenna output 1
6	VSSA	I	Ground for full bridge drivers
7	ANT2	O	Antenna output 2
8	VDDA	I	Voltage supply for full bridge drivers
9	VDD	I	Voltage supply for non-power blocks
10	OSC2	O	Oscillator output
11	OSC1	I	Oscillator input
12	VSS	I	Ground for non-power blocks
13	VSSB	I	Ground for PLL
14	SCIO	O	Data output to microprocessor
15	FSEL	I	Control input for frequency selection
16	TXCT	I	Control input for microprocessor

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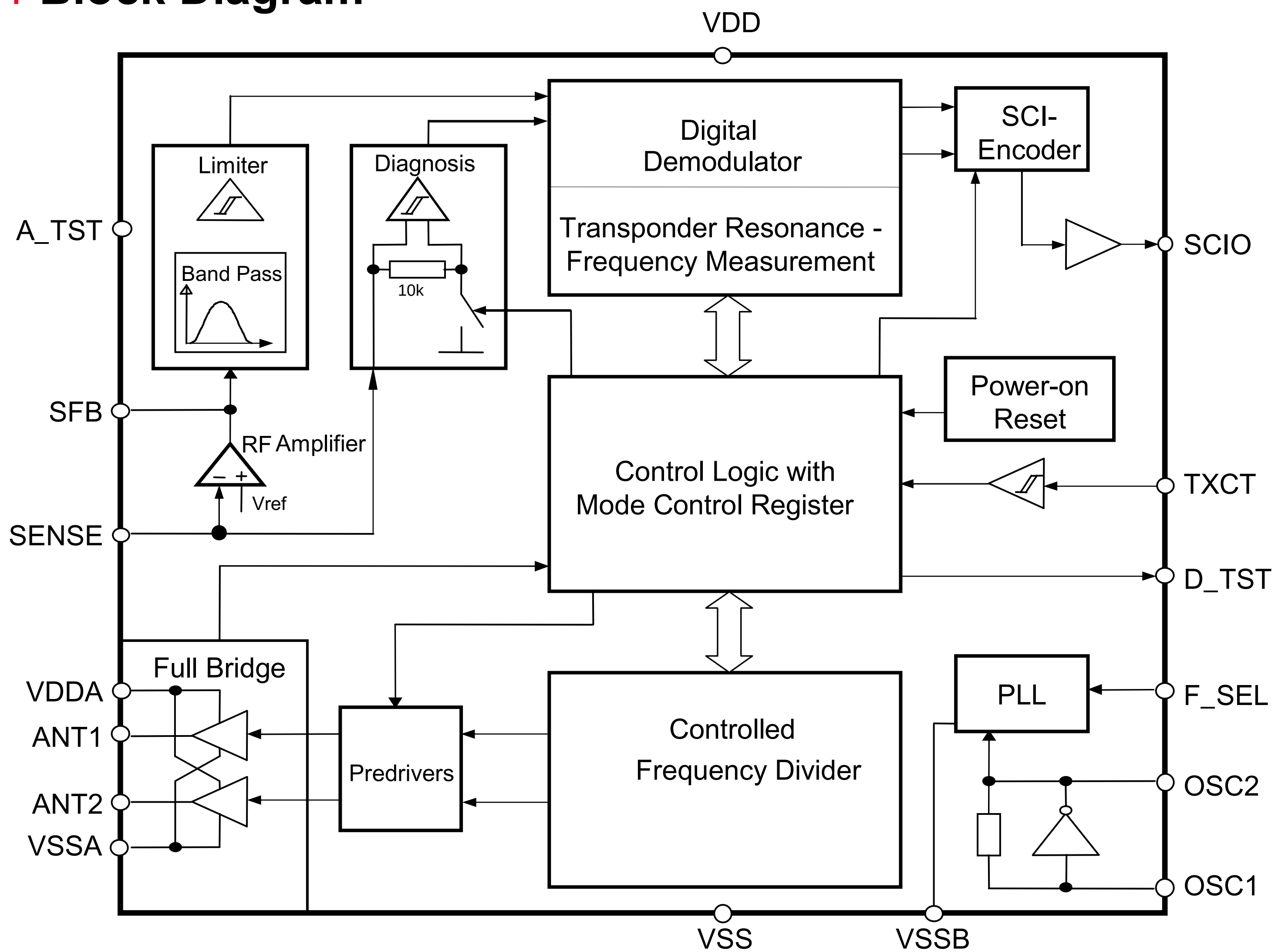
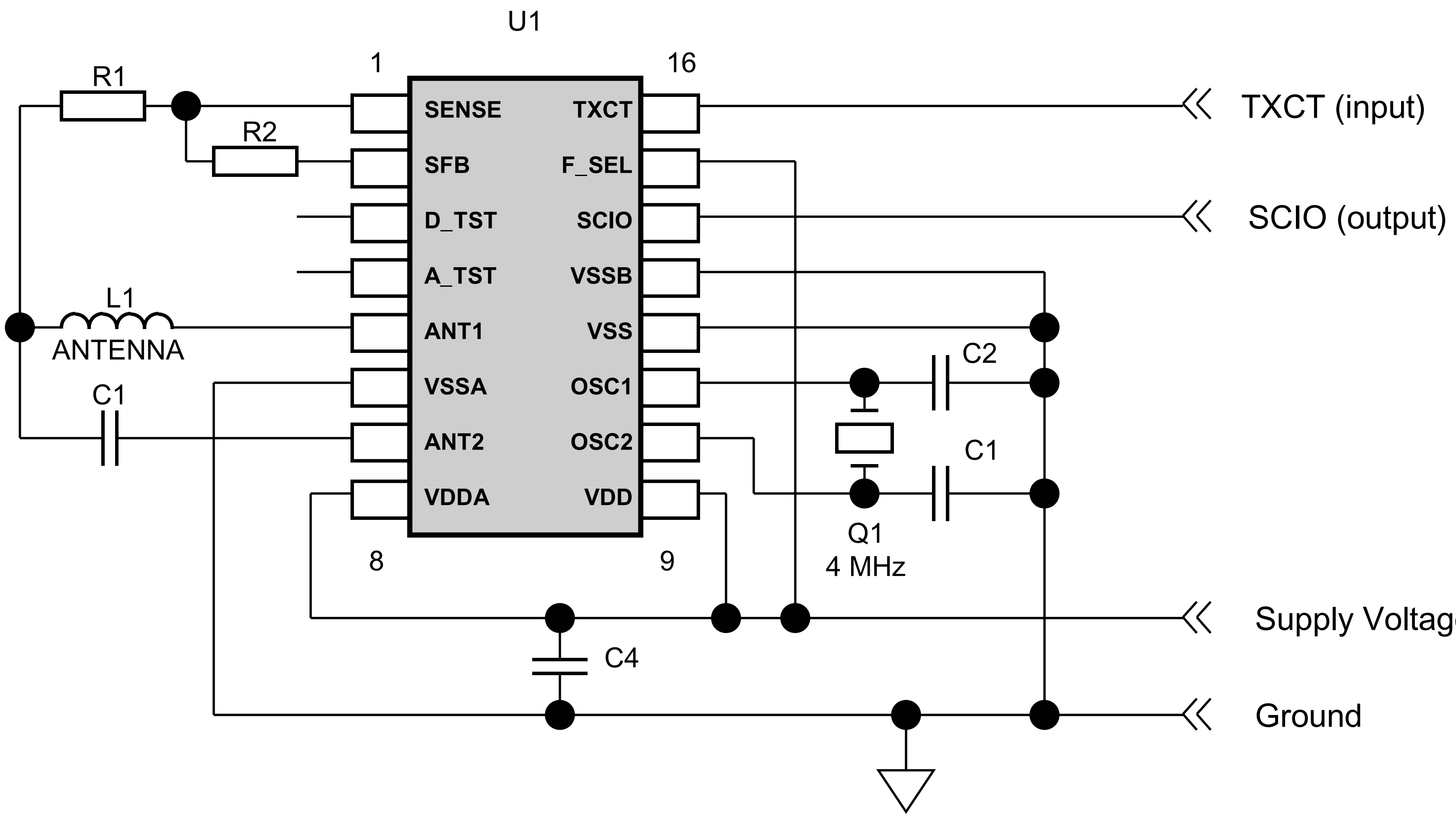
4 Block Diagram



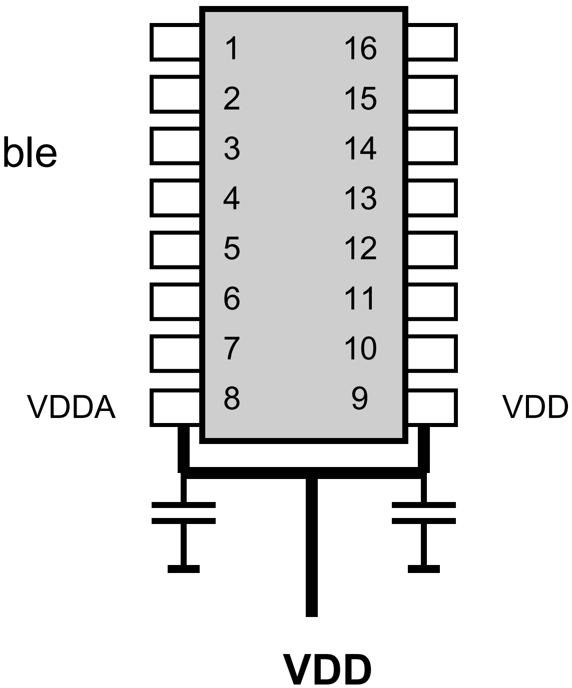
4 Generic Circuit Diagram



Transceiver IC Integration

4 Power Supply and Blocking Capacitance

- To prevent uncontrolled radiation it is recommended to connect the supply voltage symmetrically to VDDA and VDD
- Connect the blocking capacitors as close as possible to the supply pins
- Tantalum capacitors are recommended



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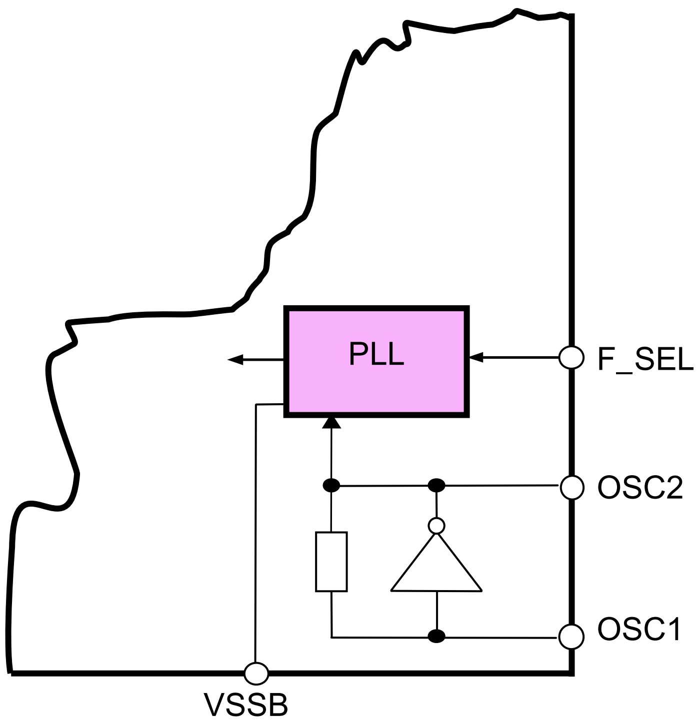
4 Oscillator - PLL



– If a Ceramic Oscillator is to be used, one with an internal load capacitance of around 56 pF is recommended
– An external oscillator signal can be fed into OSC1. OSC2 has to be left open - a decoupling capacitor is recommended.

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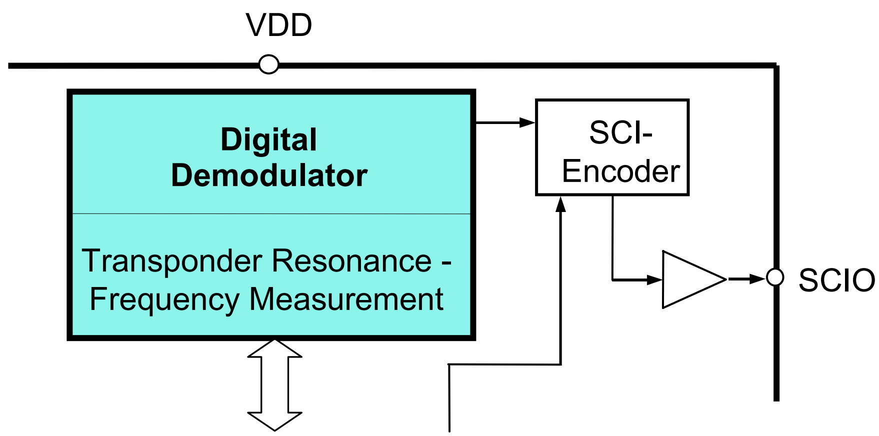
4 The Digital Demodulator



- The input frequency is measured by counting the oscillation clock for the time period of the input signal.
- The demodulator distinguishes between the high-bit frequency and the low-bit frequency by the shift values and **not** by the absolute values.
- The threshold between the high-bit and the low-bit is defined as 6.5 kHz lower than that measured for the low-bit frequency
- After the charge phase, the transponder response frequency is measured to determine the counter state for the low-bit and high-bit threshold

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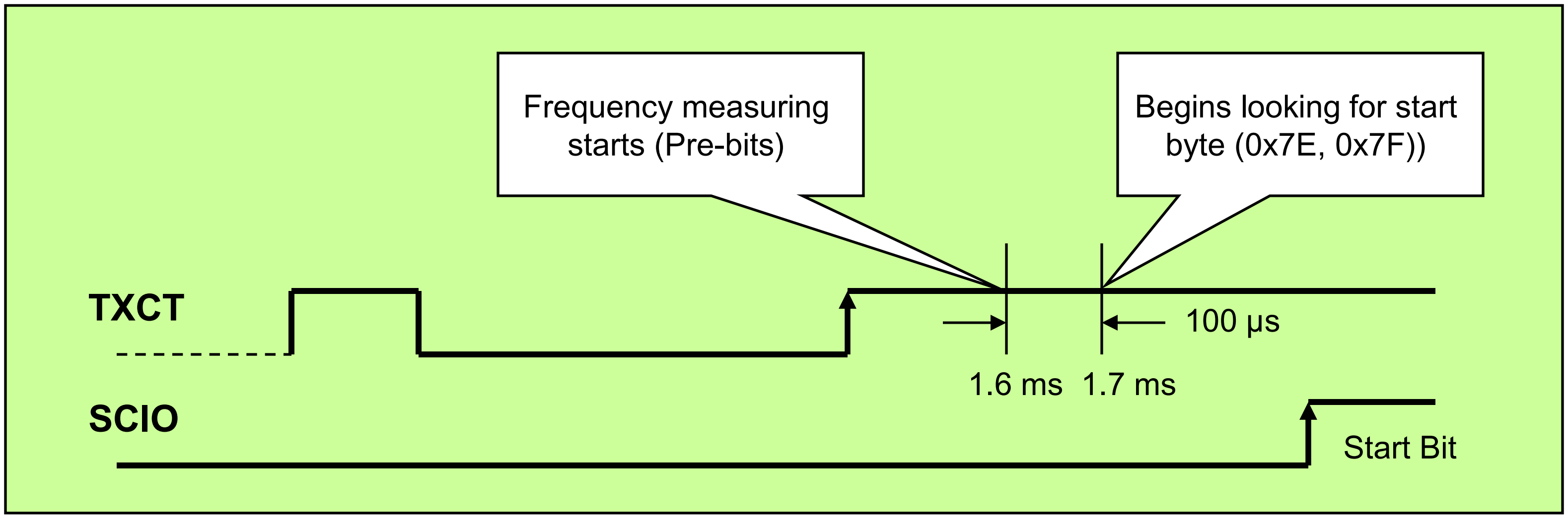
4 Transponder Resonance Frequency Measurement

– When TXCT goes high, the module enters the read phase



– 1.6 ms after TXCT goes high, an internal measuring cycle of 100 µs will start to measure the low bit frequency of the 16 transponder pre-bits.

– 1.7 ms after TXCT goes high, the IC starts looking for a valid start byte.

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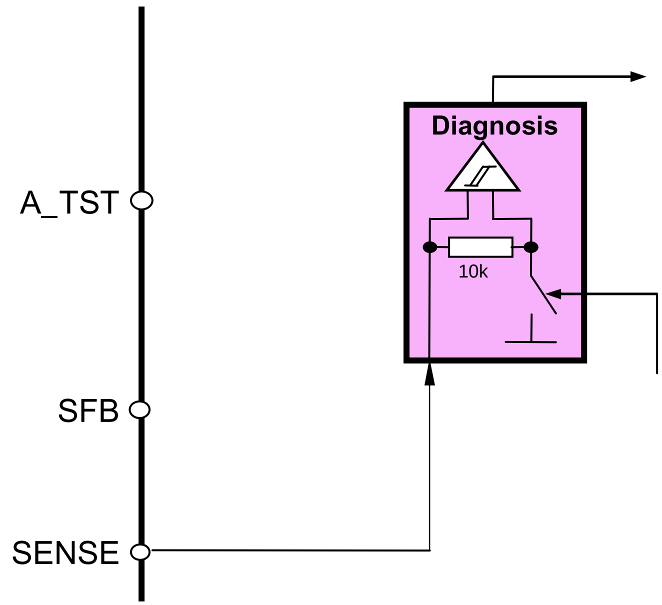
4 Diagnostics Byte



– The diagnostics byte is sent 2 ms after the start of the charge phase
  - » If normal antenna operation is detected then **0xAF** is sent
  - » If no antenna oscillation is detected or a short detection occurs, then **0xFF** is sent

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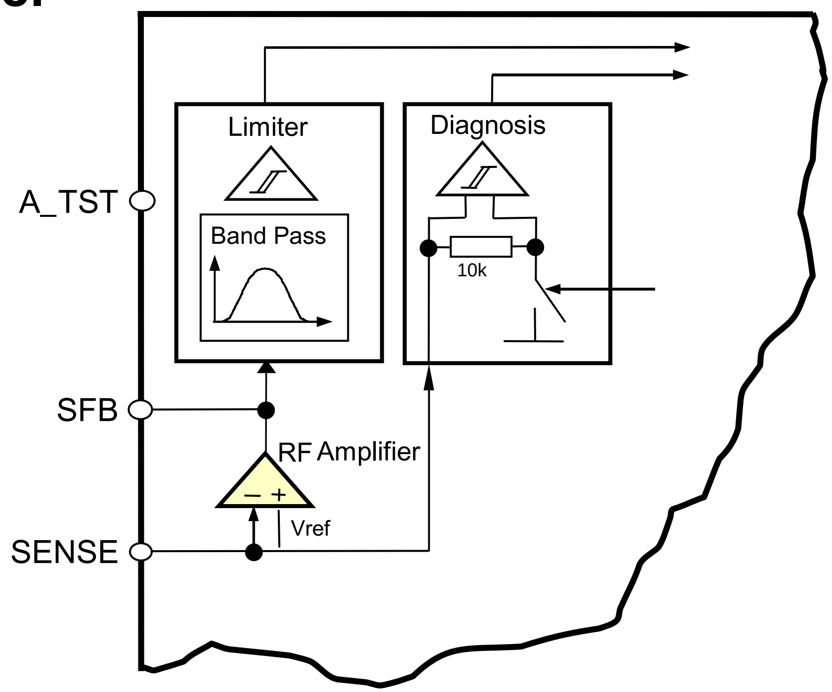
4 RX Amplifier



- The OP Amp has a fixed internal voltage reference
- A voltage gain of 5 is controlled by external resistance

$$G = \frac{R2}{R1} \qquad \frac{150k}{47k} = 3.19$$

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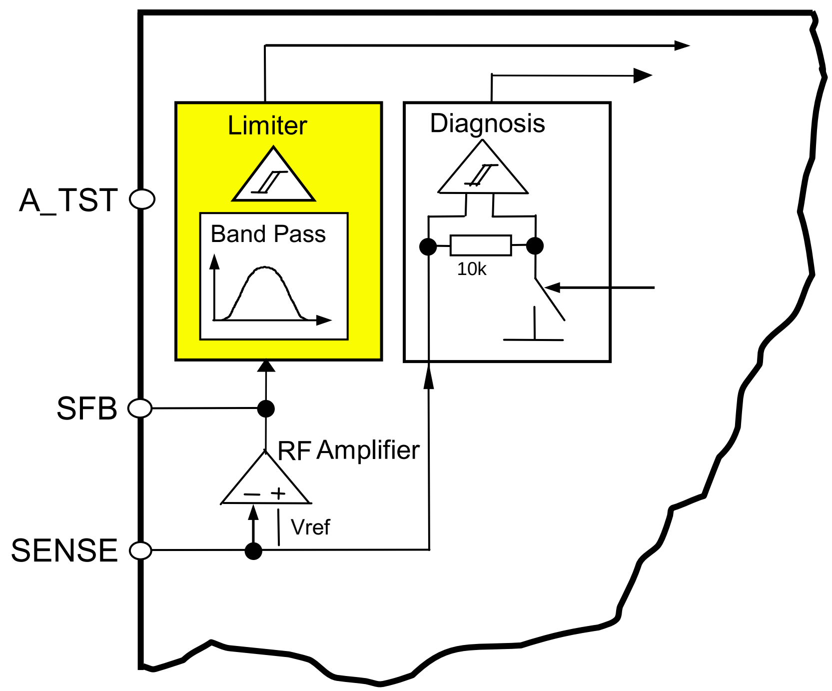
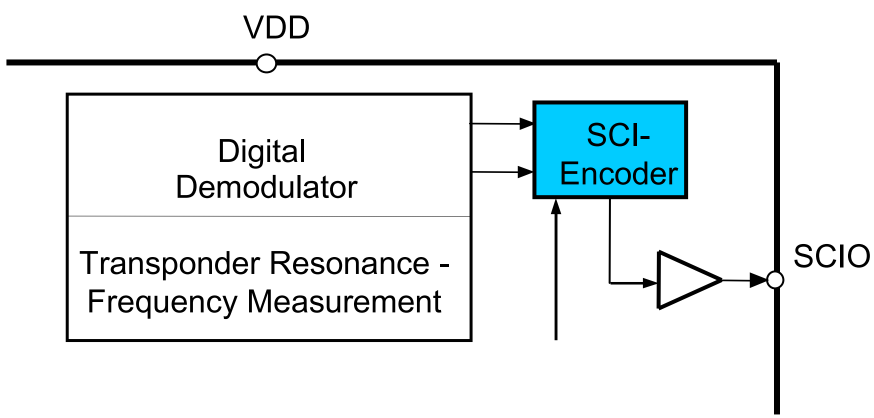
4 Band-Pass Filter & Limiter



- No external components required for filtering and amplification
- The analog sine-wave is converted to a digital signal
- High gain - at least 1000

Transceiver IC Integration

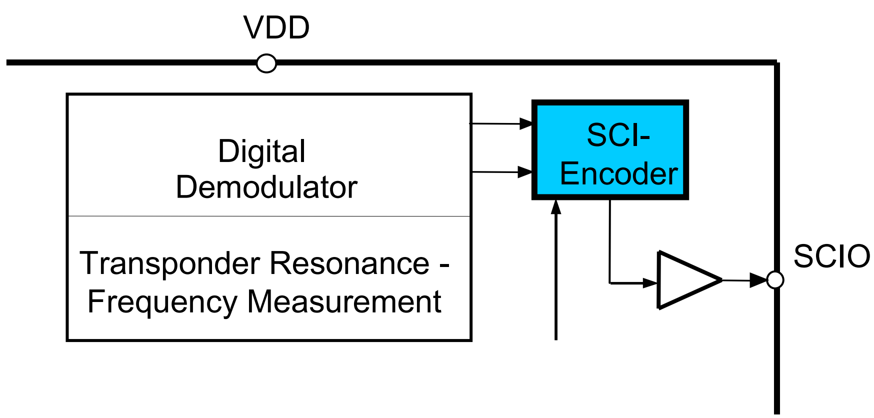
4 SCI Encoder for Data Transmission to the Controller



- An 8-bit shift register is used to buffer and send the received data byte-wise to the micro controller (**L**east **S**ignificant **B**it first)
- In Synchronous Mode, a high state at the SCSI output indicates that a new byte is ready to be transmitted
- The transmission rate is 15625 baud (in asynchronous mode) with 1 start byte (high) and 1 stop byte (low).

Transceiver IC Integration

4 SCI Encoder for Data Transmission to the Controller (2)



– The Start-Byte is the first byte sent to the microcontroller.

– Data bits at the SCIO output are inverted compared with the data from a transponder. Typical transponder values:

  » R/O Transponder = 0x81 (0x7E inverted)

  » R/W Transponder = 0x01 (0xFE inverted)

  » DST Transponder = 0x81 (0x7E inverted)

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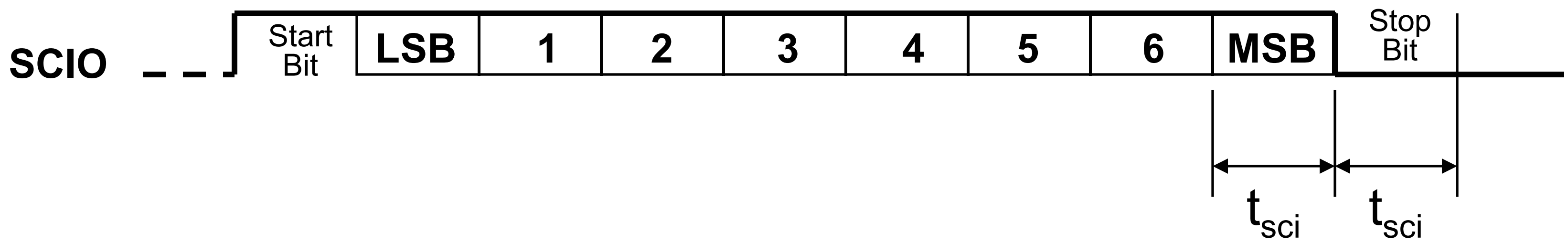
4 **SCIO Asynchronous Transmission - Timing diagram**



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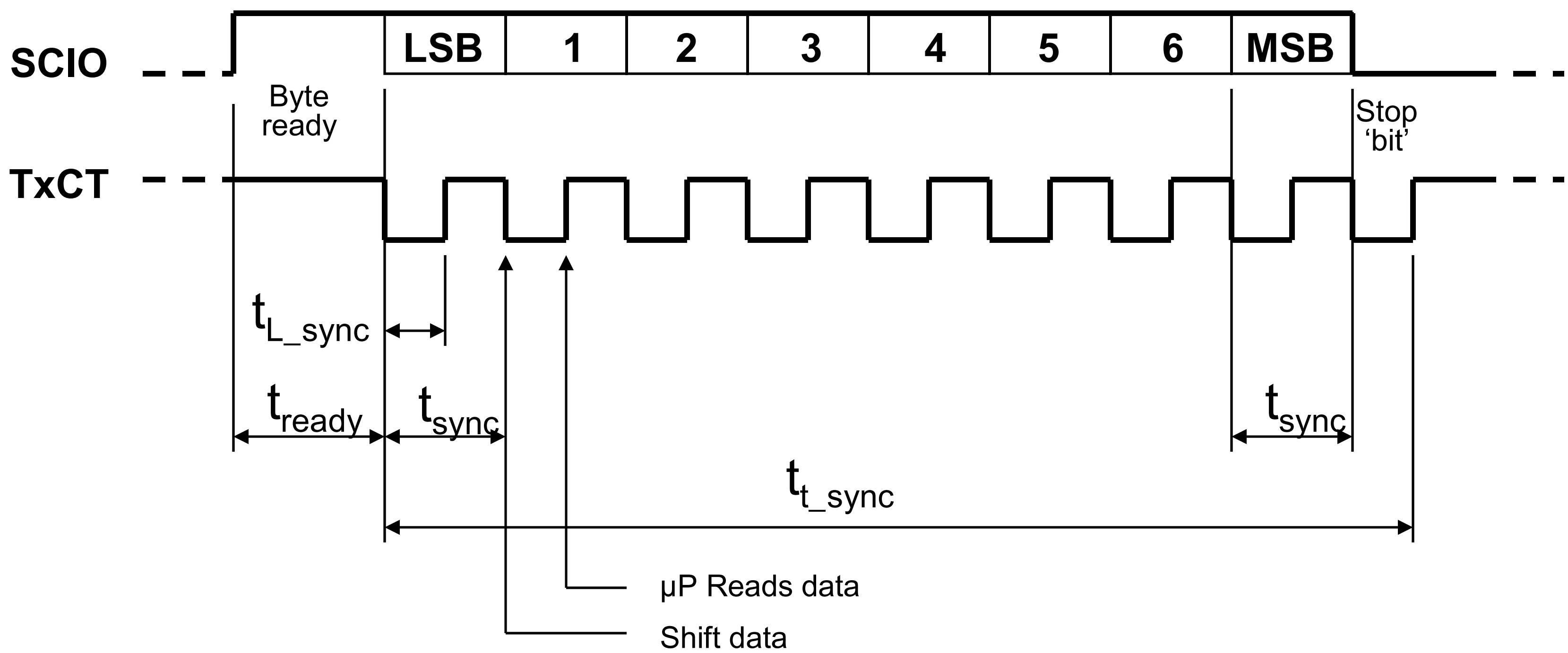
4 SCIO Synchronous Transmission - Timing diagram



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4 SCIO in Synchronous Transmission Mode

- The SCI encoder can be switched into synchronous transmission mode by setting the SCI_Sync bit in the Mode Control Register (MCR)
- The micro-controller has to clock out the data bytes by sending 8 clock signals to the TXCT input
- A high state on the SCIO indicates that a new byte is ready to be transmitted.
- The advantage of synchronous transmission:
  - » Higher speed of the byte transmission

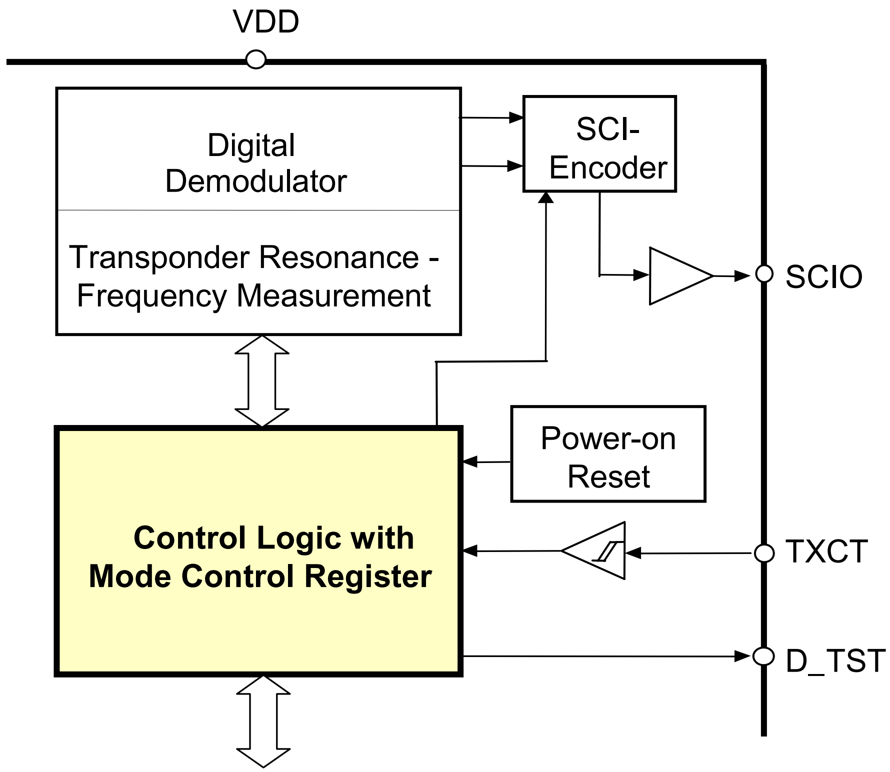
    Minimum clock period of 4µs x 8.5 = 34 µs per byte

Transceiver IC Integration

4 **Mode Control Register** (MCR)

– By writing to the MCR the mode of operation of the IC can be changed.

– The options include:
  - » Asynchronous/ Synchronous data
  - » Frequency changing
  - » Demodulator threshold adjustment
  - » Test Mode



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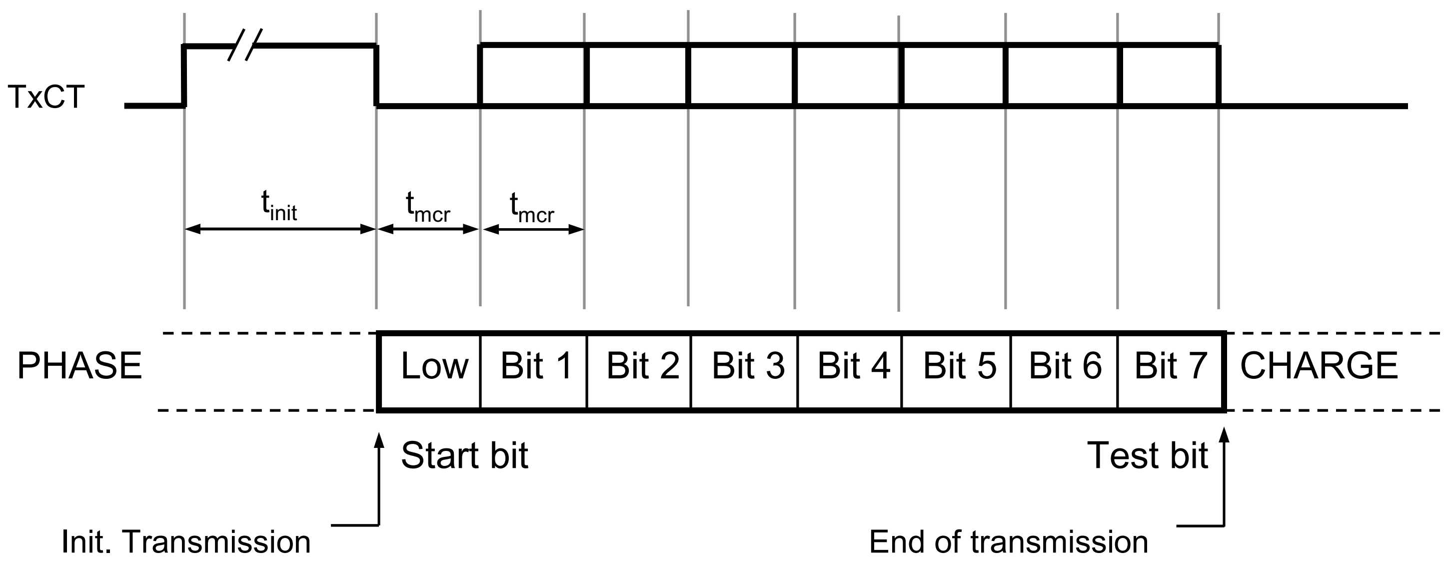
4 Timing Diagram: Mode Control Register Write Protocol



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4 **7-bit Mode Control Register** (MCR)

Bit 0	Start Bit	0	Start bit is always LOW
Bit 1			Frequency selection/ Threshold adjust
Bit 2			Frequency selection/ Threshold adjust
Bit 3			Frequency selection/ Threshold adjust
Bit 4			Frequency selection/ Threshold adjust
Bit 5	SCI_Sync	0 (default)	Asynchronous data transmission
		1	Synchronous data transmission
Bit 6	RX_AFC	0 (default)	Automatic demodulator threshold adjustment
		1	Demodulator threshold defined by bits 1~4
Bit 7	Test_Bit	0 (default)	No further bytes.
		1	Further bytes follow (Special test modes)

– The first 4 bits in a high state causes the IC to automatically adjust the carrier frequency to the transponder resonant frequency
– Other combinations allow individual frequency selection by using the division factors 114 ~ 124 (default is 119)

Transceiver IC Integration

4 **Frequency Selection** (MCR)

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Division Factor	Notes
	0	0	0	0	119	Division factor selected by µC - Default
	1	0	0	0	114	Division factor selected by µC
	0	1	0	0	115	Division factor selected by µC
	1	1	0	0	116	Division factor selected by µC
	0	0	1	0	117	Division factor selected by µC
	1	0	1	0	118	Division factor selected by µC
	0	1	1	0	119	Division factor selected by µC
	1	1	1	0	120	Division factor selected by µC
	0	0	0	1	121	Division factor selected by µC
	1	0	0	1	122	Division factor selected by µC
	0	1	0	1	123	Division factor selected by µC
	1	1	0	1	124	Division factor selected by µC
	1	1	1	1	Auto	Division factor selected automatically

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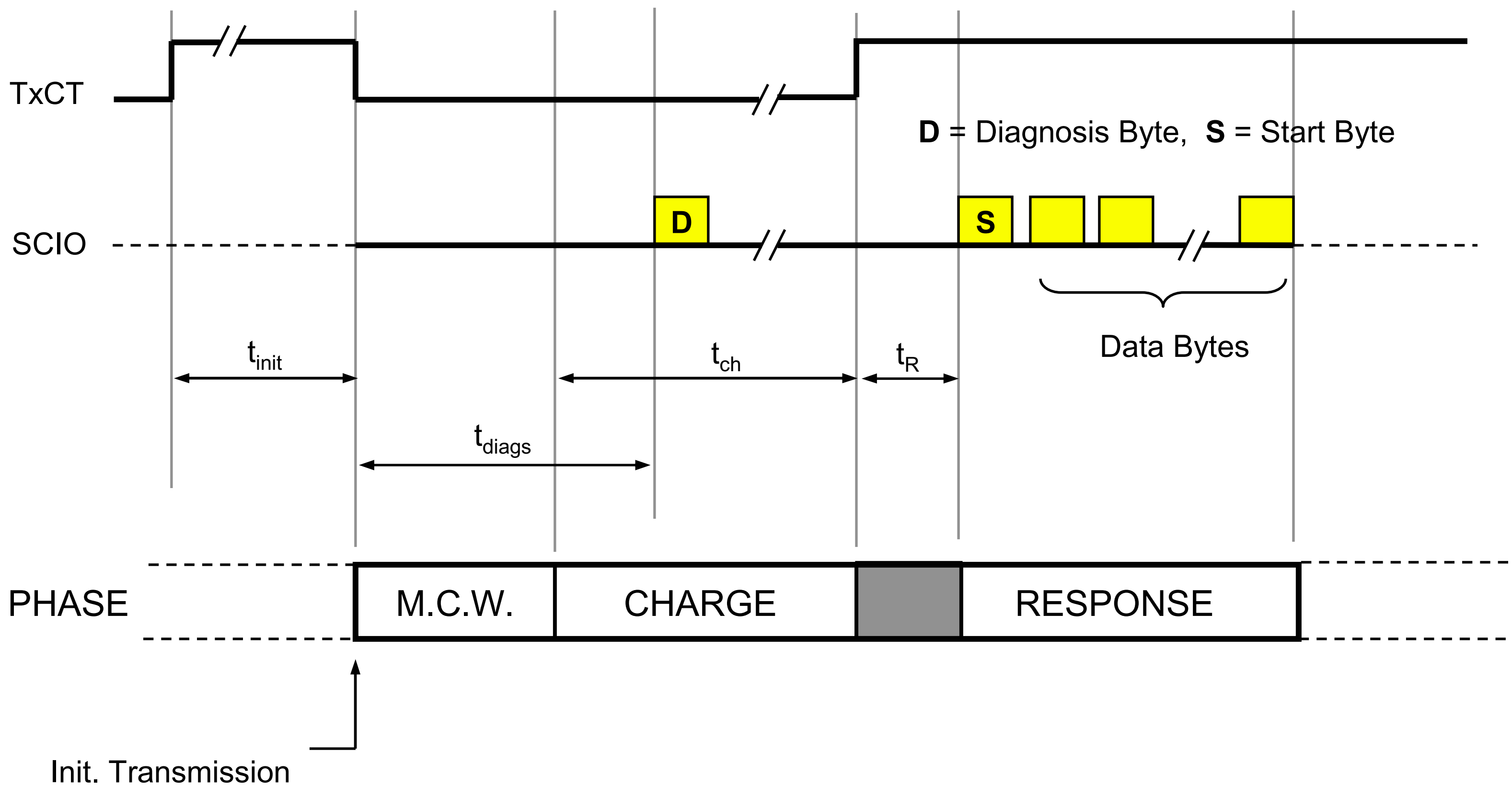
4 Timing Diagram: Default mode - No write to MCR



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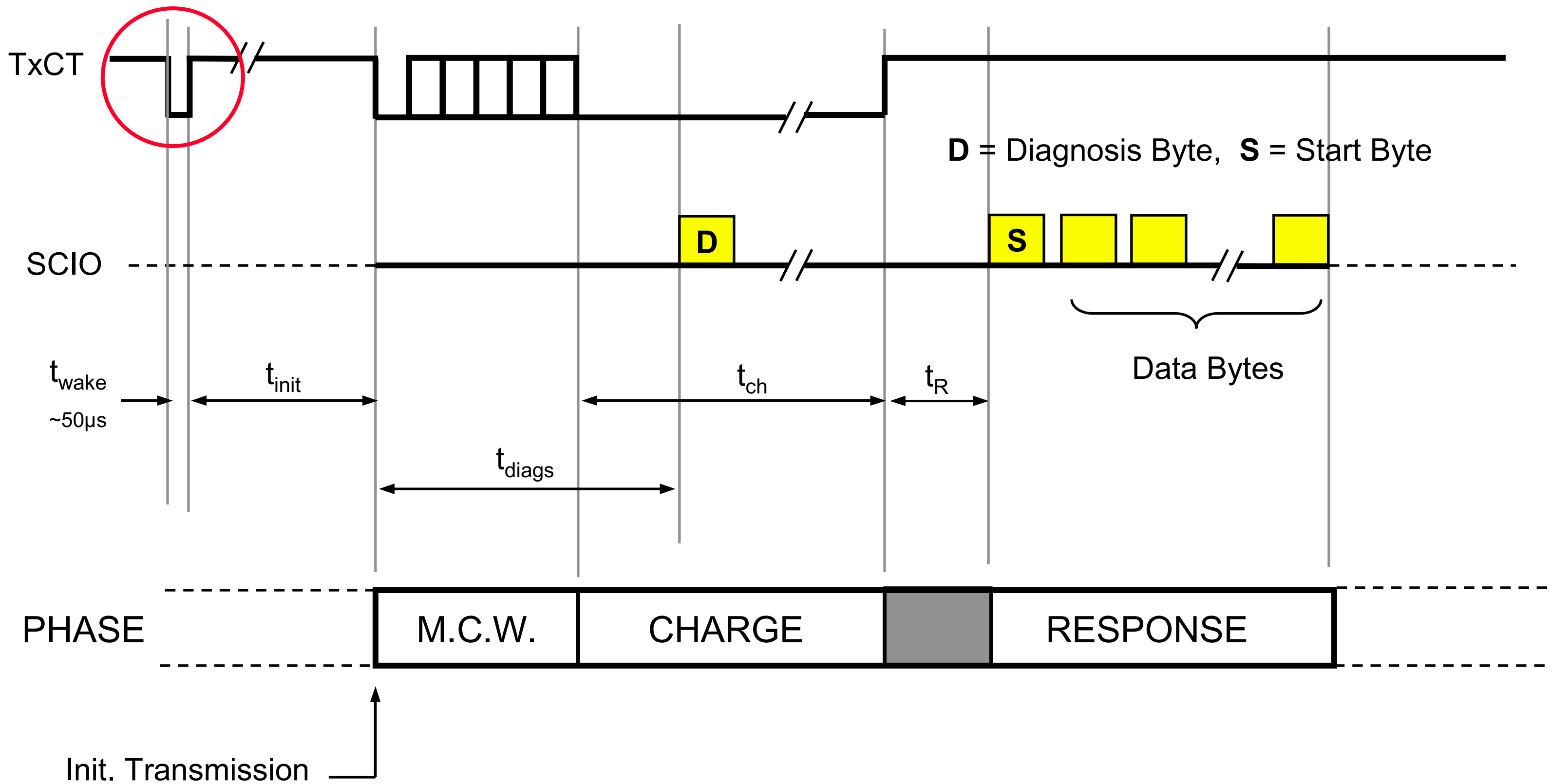
4 Timing Diagram: R/O mode - With write to MCR



NOTE: For correct writing to the MCR, it is essential to know if the IC is in IDLE or SLEEP mode

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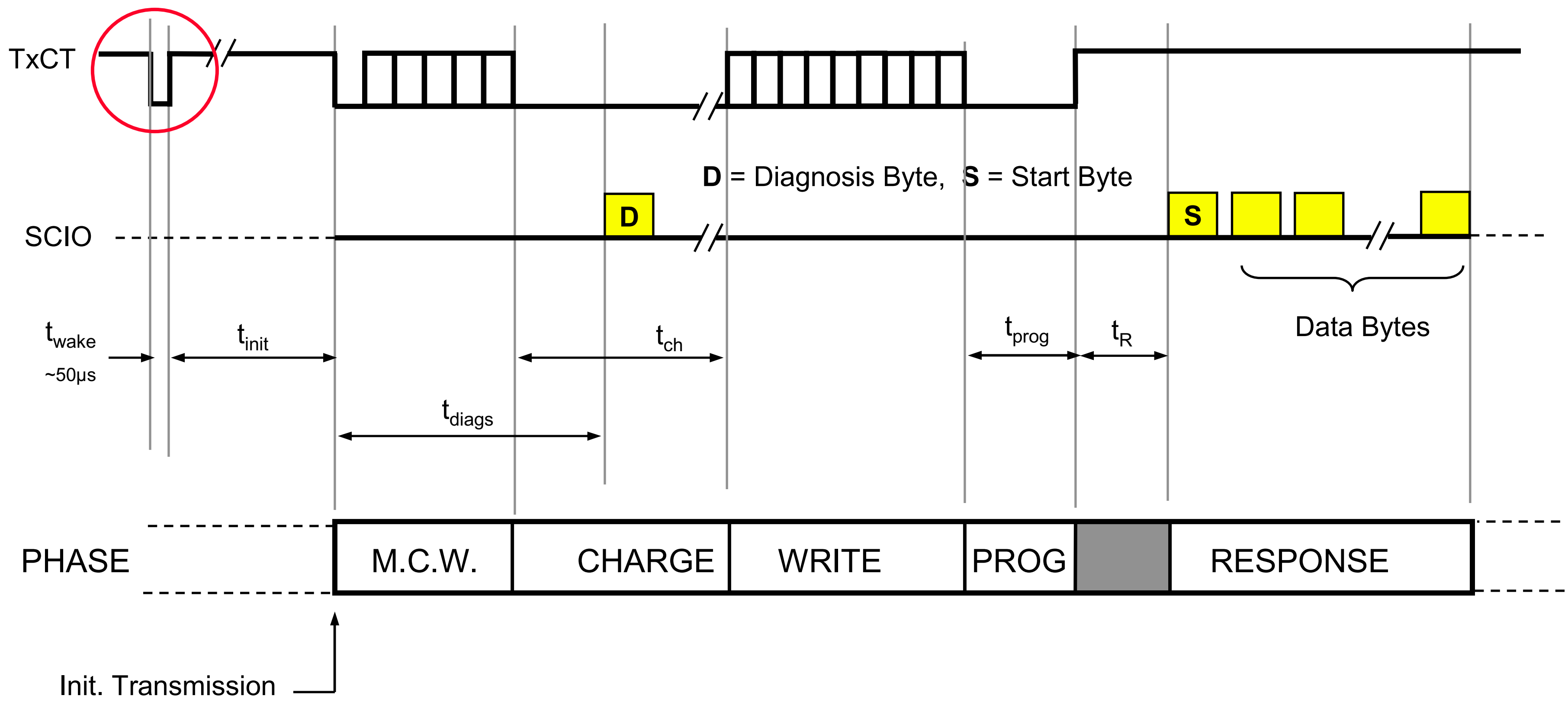
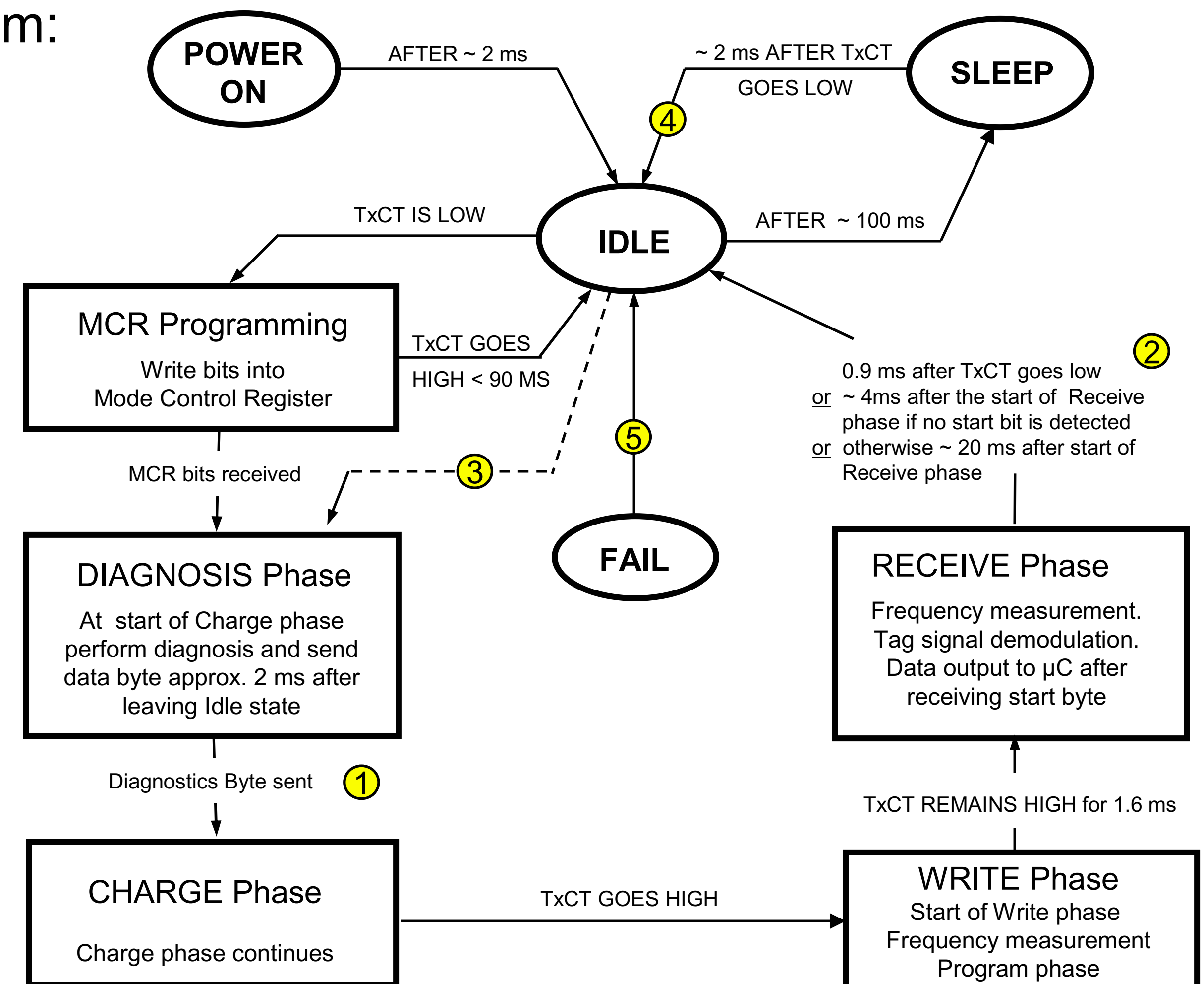
4 Timing Diagram: R/W mode - With write to MCR



NOTE: For correct writing to the MCR, it is essential to know if the IC is in IDLE or SLEEP mode

Transceiver IC Integration

4 State Diagram:



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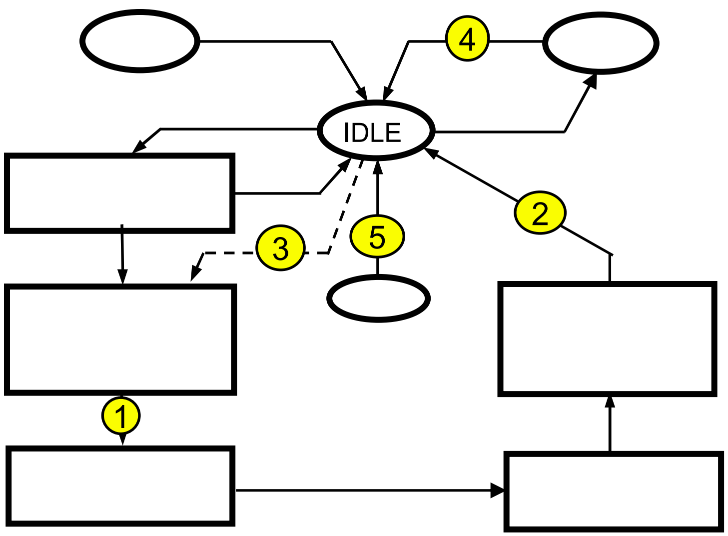
4 State Diagram Notes:



Notes:

1. In SCI synchronous mode, this transition always occurs approximately 3 ms after leaving Idle state. The diagnostics byte transmission should have completed.

2. A falling edge on TxCT interrupts the Receive phase after a delay of 0.9 ms. TxCT must remain low for at least 128 µs. If TxCT is still low after the 0.9 ms delay, the IC will go to Idle mode and then directly to the diagnostics phase 1 clock cycle later (Dotted line 3)

3. This transition only occurs in case 2 above.

4. A falling edge on TxCT interrupts the Sleep state. Only default mode is fully supported when starting an operation from Sleep with only one falling edge on TxCT (because of the 2 ms delay). For proper TxCT programming, TxCT has to return to high and remain high during this delay

5. Idle mode is the next state in the case an undefined state. (failsafe state machine)

Documentation

4 Guidelines

– TMS3705A Data Sheet	[Rev 1.0 - June 1999]
– Application Note	[11-07-26-001. Oct 1999]
– DST Reference Manual	[11-09-21-029. Dec 1998]
– DST Sequence Control Specification	[24-06-05-005. Jun 1996]
– DSP Algorithm & SW Requirements	[24-09-05-012. Oct 1995]
– Immobiliser Systems Design Guide	[Rev .01 Jan 1996]
– Tricks and Hints for System Evaluation	[Ver 2.0 Sept 1999]